Chapter 16: MOSFETS

* The most important mosfet for digital ICs is the silicon N-channel enhancement-only transistor
* This device has superior properties to those of the corresponding P-channel mosfet due primarily to the higher mobility of electrons
* The enhancement-only Mosfet is normally off when no voltages are applied making these devices devices ideal for digital logic circuits.
* Both NMOS & CMOS digital IC families using silicon are are used extensively in VLSI & ULSI circuits because of
  1. the typically small size of Mosfets compared with BJTs
  2. lower power dissipation.

Metal gate N-channel Mosfets

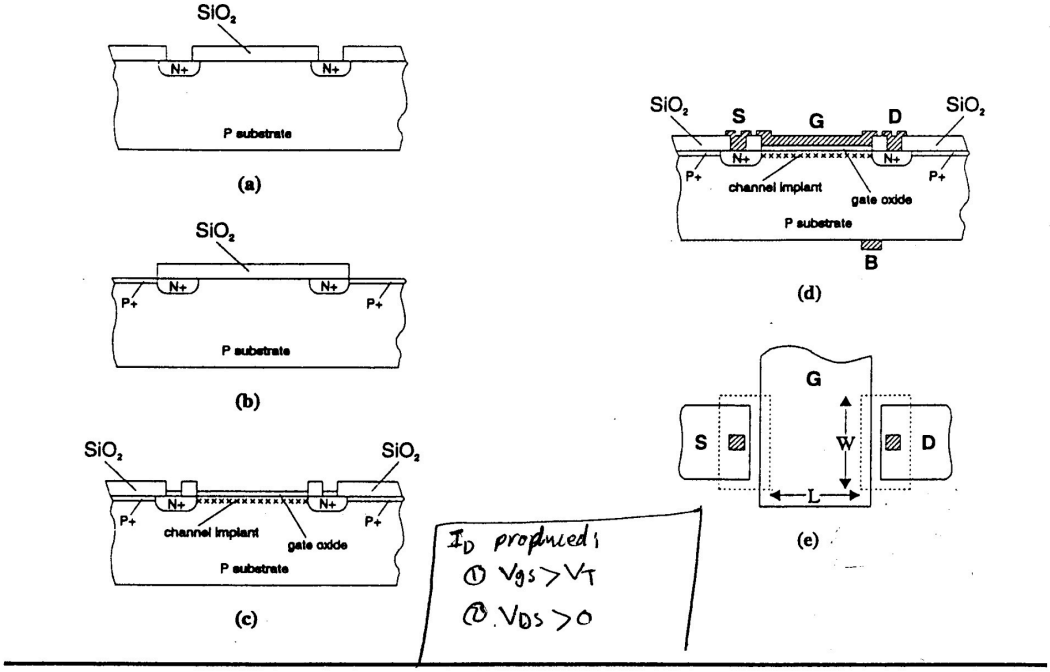


FIGURE 16.1 Basic Processing Sequence for Silicon N-channel MOSFET with Metal Gate: (a) Source/drain N+ diffusion/implant, (b) Channel stop P+ implant, (c) Channel implant and gate oxide growth, (d) Metal deposition and etch, (e) Layout defining channel width W and length L

Silicon gate N-channel Mosfets

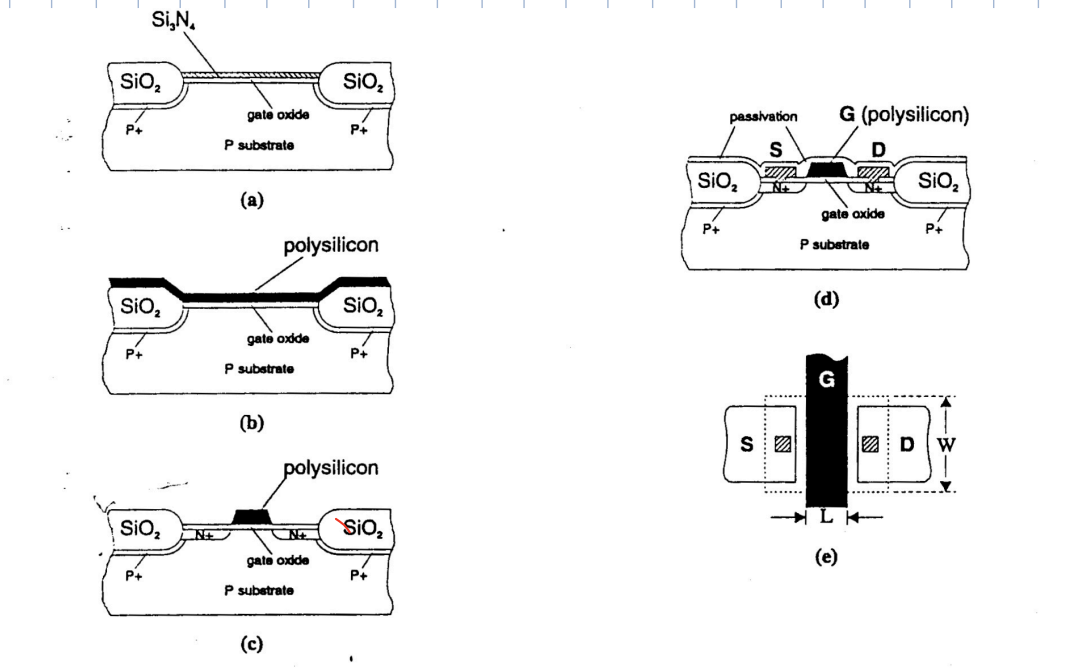
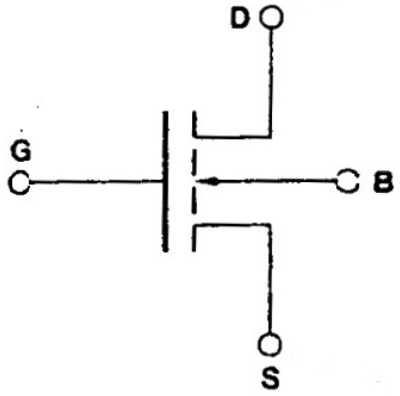


FIGURE 16.2 Basic Processing Sequence for Silicon N-channel MOSFET with Polysilicon Gate: (a) Gate oxide growth, Si_3N_4 growth and etch, channel stop implant, thick oxide growth, (b) Si_3N_4 removal, polysilicon deposition, (c) Etch polysilicon and source/drain N+ implant, (d) Metal deposition and etch and passivation layer deposition, (e) Layout defining channel width W and length L

Mosfet modes of operation

* The circuit symbol for the nMos is shown in the figure to the right



Threshold voltage

* In order for drain current to flow from drain to source in nMOS there is two conditions

  1. $V_{GS} > V_T$
  2. $V_{DS} > 0$

* The threshold voltage is dependent upon the physical dimensions and parameters of the MOS device.

* For the enhancement-only nMOS transistor the threshold voltage is +ve and for the enhancement-depletion nMos the threshold voltage is -ve.

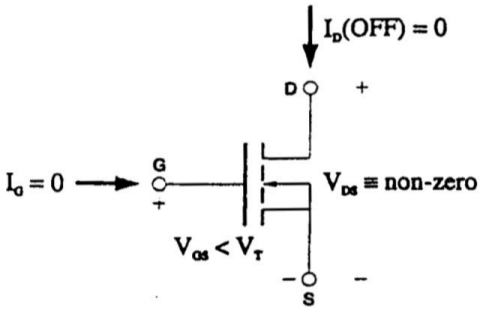
* For pMos devices the threshold voltage is opposite in sign to the corresponding nMOS

TABLE 16.1 Signs of MOSFET Threshold Voltage

	NMOS	PMOS
Enhancement-only	+	−
Enhancement-depletion	−	+

Cutoff

* For nMOS device if $V_{GS} < V_T$ then the nMOS device is in cutoff mode of operation & $I_D = 0$.



(a) cutoff mode

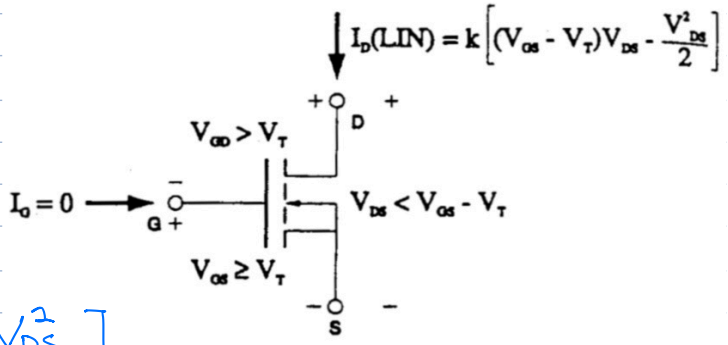
Linear Mode.

* As V_{GS} is increased above V_T a drain current conducts for $V_{DS} > 0$

* For nMos device to be in linear mode of operation there is two conditions

$$V_{GS} > V_T$$

$$V_{DS} \leq V_{GS} - V_T$$



(b) linear mode

thus

$$I_D(lin) = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

where $k \equiv$ transconductance parameter.

Saturation mode

* As V_{DS} is increased, there is two conditions to enter saturation

① $V_{GS} > V_T$

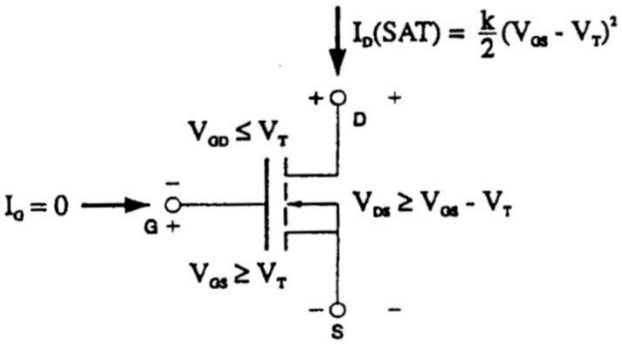
② $V_{DS} \geq V_{GS} - V_T$

Thus: $I_D(sat) = \frac{k}{2}(V_{GS} - V_T)^2$

The expression indicates that the saturation drain current has no dependence on V_{DS}. but this is not entirely true in the actual case and the variation with V_{DS} is sometimes accounted for by specifying a channel-length modulation λ

$$I_D(sat) = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

where $\lambda \equiv$ channel-length modulation



(c) saturation mode

Family of curves

* For nMOS I_D is plotted versus the voltage V_{DS} with V_{GS} as a parameter
* Note that unlike the family of curves for the BJT. I_D does not increase approximately linearly for equal increments in the input parameter V_{GS}
* The linear mode of operation is to the left of the $V_{DS} = V_{GS} - V_T$ & the saturation mode is to the right & the cutoff mode of operation is defined to be the region where all currents are zero and $I_D = 0$.

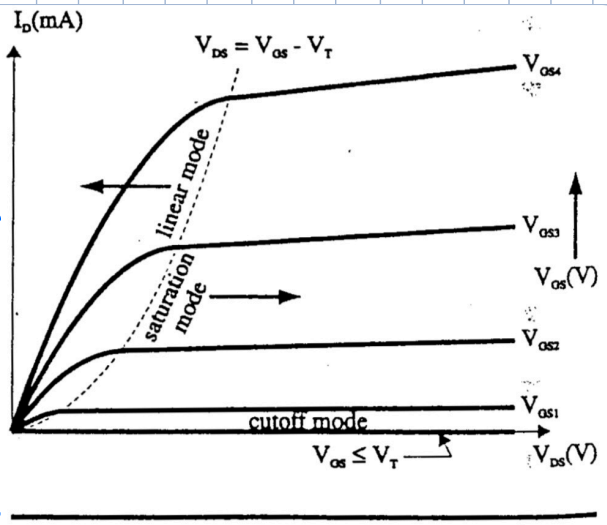


FIGURE 16.4 MOSFET Family of I_D versus V_{DS} Curves with V_{GS} as a Parameter

* Note that no reverse-active mode in FET because of symmetry in fabrication.

* Which way is Up?
* Due to the inherent symmetric fabrication of Mosfets the source & drain are interchangeable, thus there is no RA mode of operation for Mosfets.
* The desired source region is connected to the body (substrate) and this therefore defines which end of the channel is the source
* Not all Mosfets in ICs can have their sources connected to the body. The drain is then defined as the channel side region at higher voltage while the source is the channel side at a lower voltage
* $V_{DS} > 0$ is always true for an active nMOS & if V_{DS} changes sign the source & drain are interchanged.

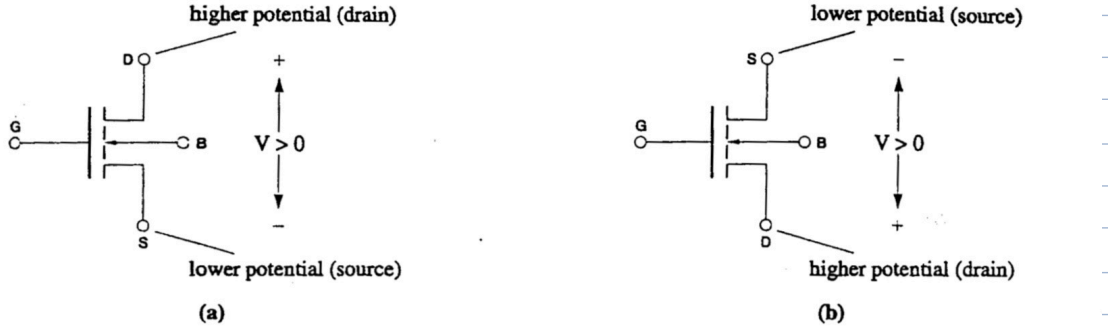


FIGURE 16.5 Determination of Drain and Source for Symmetric NMOS, i.e. body not tied to either end of channel

Example 16.1 ***NMOS Drain Current Calculation***

An NMOS transistor has $k = 20\mu A/V^2$ and $V_{T0} = 1$ V. Assume $\gamma_L = 0$. Find the drain current for the edge of saturation (i.e. $V_{DS} = V_{GS} - V_T$) for $V_{GS} = 3$ V using both the linear and saturation drain current expressions.

@ EOS $\quad V_{DS} = V_{GS} - V_T = 3 - 1 = 2V$

$$I_D(lin) = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] = 20\mu\left[(3-1)(2) - \frac{(2)^2}{2}\right]$$

$$I_D(lin) = 40\mu A$$

$$I_D(sat) = \frac{k}{2}(V_{GS} - V_T)^2 = \frac{20\mu}{2}(3-1)^2 = 40\mu A$$

* Note that $I_D(lin) = I_D(sat)$ which was expected @ EOS.

Mosfet transconductance parameter

* k has units of A/V^2 & the magnitude of k for a Mosfet is a direct function of the physical characteristics of the device

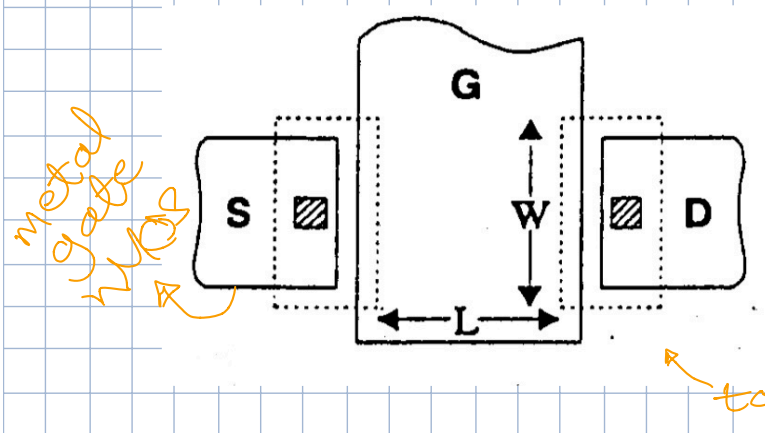
Device transconductance parameter $\equiv$ k

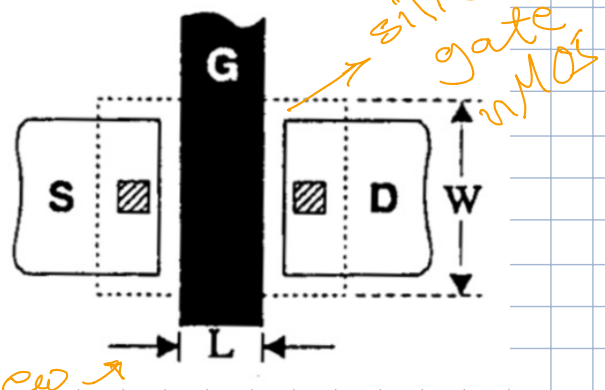
* The parameter k referred to as the device transconductance parameter of a Mosfet is related to the channel width & length by

$$k = k' \frac{W}{L}$$

* k' is referred to as the process transconductance parameter

* k is called the device transconductance parameter because of its relationship to the channel width & length





Process transconductance parameter $\equiv k'$

* The process transconductance parameter is determined from

$$k' = \mu C'_{ox}$$

$\mu \equiv$ the mobility

$C'_{ox} \equiv$ the gate oxide capacitance per unit area

k' is called the process transconductance parameter because its value determined by the fabrication process & all Mosfets on a given IC have the same k'

* For nMos typically $\mu_n = 580\ cm^2/V.s$
* For pMos the hole mobility is typically $\mu_p = 230\ cm^2/V.s$

Gate capacitance per unit area $\equiv C'_{ox}$

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad \text{(per unit area)}$$

$\epsilon_{ox} \equiv$ the premitivity of the gate oxide & is related to the ~ ~ vacuum by the relation

$$\epsilon_{ox} = k_{ox} \times \epsilon_0 = 3.9 \times \epsilon_0$$

$k_{ox} \equiv$ the dielectric constant of SiO_2

For SiO_2: $\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$

Mosfet threshold voltage

* The threshold voltage is the critical gate bias voltage at which conduction between the source & drain can be initiated

$$I_D(off) = 0 \quad (V_{GS} < V_T)$$

Zero body bias threshold voltage

* The threshold voltage of a typical silicon Mosfet depends upon the device geometry as well as material parameters

V_T with $V_{SB} = 0$

$$V_{TO} = -|\phi_{MS}| - |2\phi_F| - \left|\frac{Q'_B}{C'_{ox}}\right| - \left|\frac{Q'_{SS}}{C'_{ox}}\right| + \frac{Q'_I}{C'_{ox}}$$

$\phi_{MS} \equiv$ Difference of gate-metal & silicon work functions [V]

$\phi_F \equiv$ surface potential [V]

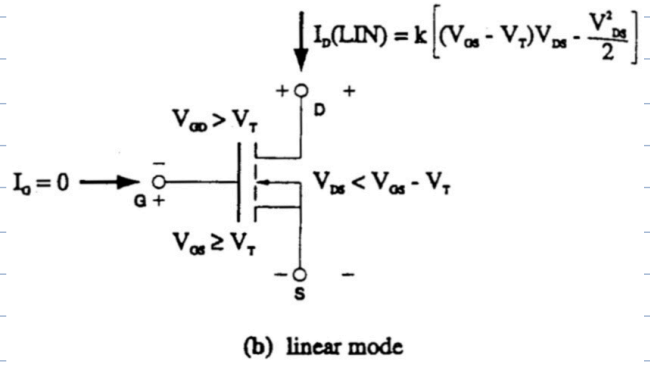
$Q'_B \equiv$ surface depletion region charge per unit area [c/cm^2]

$Q'_{SS} \equiv$ surface state charge per unit area associated with $Si-SiO_2$ interface states [c/cm^2]

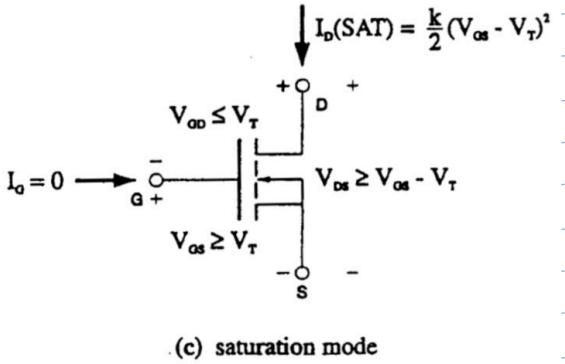
$Q'_I \equiv$ Ion implantation into the channel region [c/cm^2]

* Note that all terms are negative except for the last term. Q_I represents ion implantation into the channel region that is necessary to make V_{TO} positive also the primes indicate per unit area.

Body bias dependance of threshold voltage



(b) linear mode

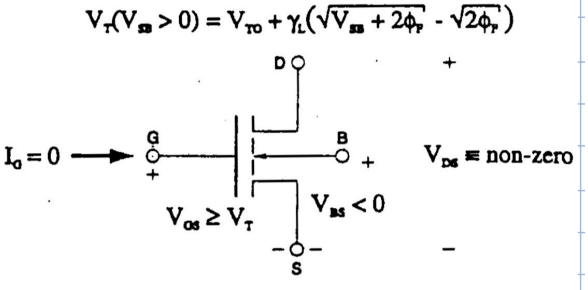


(c) saturation mode

* The figures shows the body (or substrate) connected to the source for both the linear and saturation modes of operation.

* The voltage V_{SB} is referred to as a body-bias. the presence of a body-bias voltage has the effect of shifting the threshold voltage

$$V_T(V_{SB} > 0) = V_{TO} + \gamma_L\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$



(d) body-bias effect on threshold voltage

V_{TO} ≡ zero body-bias threshold voltage

γ_L ≡ body-effect coefficient

ϕ_F ≡ the surface potential.

Example 16.2 *NMOS Threshold Voltage Calculation*

For the MOSFET of Example 16.1, calculate the threshold voltage for a body-bias of 3 V. Use $\gamma_L = 0.54\ V^{1/2}$, and $2\phi_F = 0.6$ V.

$$V_T(V_{SB}>0) = V_{TO} + \gamma_L\left(\sqrt{V_{SB}+2\phi_F} - \sqrt{2\phi_F}\right)$$

For $V_{SB} = 3V$

$$V_T = 1 + (0.54)\left(\sqrt{3+0.6} - \sqrt{0.6}\right)$$

$$V_T = 1.61V$$

P-channel Mosfet

* The modes of operation for pMOS are the same as those for nMOS
* The drain current expressions are identical in form with the voltage polarities & current directions reversed.

* cutoff ≡ $V_{SG,P} \leq -V_{TP}$

$$I_{D,P}(off) = 0$$

* Linear ≡ $V_{SG,P} \geq -V_{TP}$ &

$$V_{SD,P} \leq V_{SG,P} + V_{TP}$$

$$I_{D,P}(Lin) = k_P\left[(V_{SG,P}+V_{TP})V_{SD,P} - \frac{V_{SD,P}^2}{2}\right]$$

* saturation ≡ $V_{SG,P} \geq -V_{TP}$ &

$$V_{SD,P} \geq V_{SG,P} + V_{TP}$$

$$I_{D,P}(sat) = \frac{k_P}{2}(V_{SG,P}+V_{TP})^2 \quad \text{or}$$

$$I_{D,P}(sat) = \frac{k_P}{2}(V_{SG,P}+V_{TP})^2(1+\lambda V_{SD,P})$$

$$V_{TP}(V_{BS,P}>0) = V_{TO,P} - \gamma_P\left(\sqrt{V_{BS,P}+2|\phi_{F_P}|} - \sqrt{2|\phi_{F_P}|}\right)$$

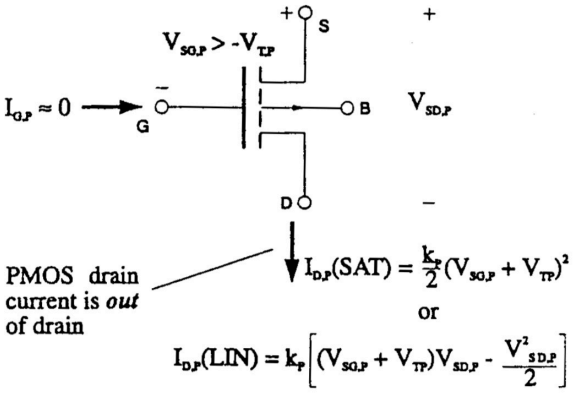


FIGURE 16.6 P-channel MOSFET, Reversal of Voltage Subscripts and Current Direction

* Note that the polarity change in voltage for pMOS is accompanied by reversing the subscripts
* The sign change in the drain current is achieved by reversing the positive current direction

Threshold voltage

* Enhancement-only $\equiv V_{TO,P} < 0$
* Enhancement-depletion $\equiv V_{TO,P} > 0$
* Body bias effect $\equiv V_{TP} = V_{TO,P} - \gamma_P \left(\sqrt{V_{BS,P} + 2|\phi_{FP}|} - \sqrt{2|\phi_{FP}|} \right)$
* Zero body-bias threshold voltage $\equiv V_{TO,P}$

Mosfets capacitances

* A capacitance exists between each pair of terminals except the source & drain.

Junction capacitances

* The capacitances C_{BS} & C_{BD} are PN junction capacitances between either the source or drain & the body (substrate).

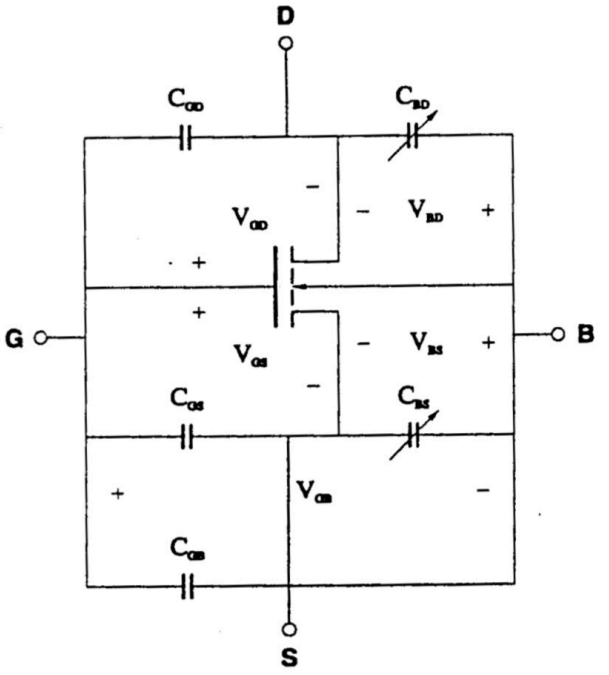


FIGURE 16.7 MOSFET Capacitances

$$C_{BS}(V_{BS}) = \frac{C_{BSO}}{\left(1 - \frac{V_{BS}}{\phi_{BS}}\right)^{m_B}}$$

$$C_{BD}(V_{BD}) = \frac{C_{BDO}}{\left(1 - \frac{V_{BD}}{\phi_{BD}}\right)^{m_B}}$$

where:

C_{BSO} & $C_{BDO} \equiv$ zero-bias junction capacitances [F]

ϕ_{SB} & $\phi_{DB} \equiv$ junction potentials (typically 0.9 to 1V)

$m_B \equiv$ grading coefficient ($m_B \approx 1/2$ or $1/3$)

Gate Oxide capacitances

* The capacitances C_{GS}, C_{GD} & C_{GB} between the gate & source, drain and body

* A simple approximation for the relationship between these capacitance values (that neglects fringing electrical fields) is that the sum of these is equal to the total gate capacitance or

$$C_{GS} + C_{GD} + C_{GB} = C_G = WL C'_{ox}$$

where:

$W \equiv$ channel width [m]

$L \equiv$ channel length [m]

$C'_{ox} \equiv$ gate capacitance per unit area of the gate dielectric [F/m^2] given by

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$\epsilon_{ox} \equiv$ permittivity of $SiO_2 = k_{ox}\,\epsilon_o = 3.45 \times 10^{-13}$ F/cm

$$\epsilon_{ox} = k_{ox}\,\epsilon_o$$

$$= 3.45 \times 10^{-13} \text{ F/cm} = 3.45 \times 10^{-11} \text{ F/m}$$

$k_{ox} \equiv$ dielectric constant of $SiO_2 = 3.9$

$\epsilon_o \equiv$ permittivity of vacuum 8.85×10^{-14} F/cm $= 8.85 \times 10^{-12}$ F/m

$t_{ox} \equiv$ gate oxide thickness

SPICE Mosfet Model

(self study to whom who concern)

CMOS devices.

* CMOS uses complementary N- & P-channel Mosfets in pairs, portions of the semiconductor surface must be N-type & nearby also P-type

* The figure to the right shows two different cross sections with complementary Mosfets that have been used to achive CMOS digital IC's

* Figure "a" starts with a p-type substrate & the N-tub at the surface is formed by diffusion/implantation.

* Figure "b" starts with the oppsite type substrate & hence the P-tub. must be manufactured into the surface.

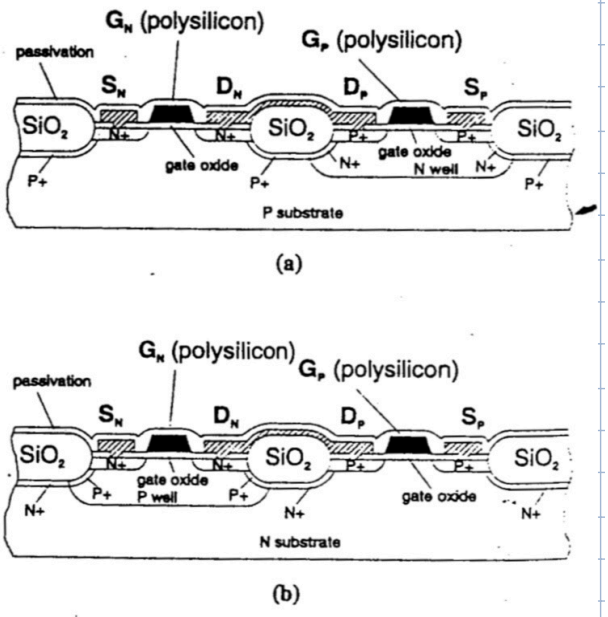


FIGURE 16.9 CMOS Cross Sections (a) N-well CMOS process: P-substrate with PMOS device built inside N-wells, (b) P-well CMOS process: N-substrate with NMOS device built inside P-wells

Twin tub CMOS process (self study)

Integrated circuit capacitors

* The usual capacitor used with silicon IC's is the metal-oxide semiconductor (MOS) parallel-plate capacitor shown in the figure

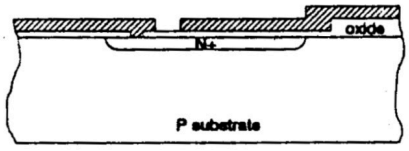


FIGURE 16.11 MOS Parallel Plate Capacitor

* The capacitance associated with this capacitor is

$$C = \frac{k_{ox}\,\epsilon_0\,A}{d} = \frac{\epsilon_{ox}\,A}{d}$$

where:

$k_{ox} \equiv$ dielectric constant of $SiO_2 = 3.9$
$\epsilon_0 \equiv$ permittivity of free space 8.85×10^{-14} F/cm
$d \equiv$ oxide thickness
$A \equiv$ overlay area of parallel plates
$\epsilon_{ox} \equiv$ permittivity of $SiO_2 = 3.45 \times 10^{-13}$ F/cm